FAA National Software Conference, May 2002
Complex Hardware (PLD/ASIC) Experiences

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Outline

- Purpose: To discuss experiences in the application of DO-178B and DO-254 for PLD and ASIC development.
  - Introduction & disclaimer
  - History
  - The many hats we wear
  - Are SW DERs value added in this area?
  - Helpful links and Information

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Introduction & Disclaimer

- This presentation presents experiences over the past 5 years surrounding the area of PLDs and their use in the development of avionics equipment.
- These experiences are not intended to imply an FAA policy or approved approach.

History

- It all started…. for me in 1987 as a Co-op writing test vectors for PLDs which were designed for Unisys mainframe computers.
- In 1998, during the development of the Boeing 777 the first Issue paper was applied to PLDs and ASICs which suggested a DO-178A+ process be used for there development.
- As a result of the 777 the Issue paper was made Generic and it is being applied on all new projects submitted to the FAA?….
- RTCA special Committee SC-180 started working on an complex electronic hardware design assurance guidance. This effort resulted in RTCA DO-254.
- 2001-2002 JAA guidance leaflet supplementing DO-254/ED-80
- GAMA draft AC as an industry response to the JAA and FAA positions and potential FAA AC invocation of DO-254 for all hardware including PLDs and ASICs. This draft AC proposes application for only levels A and B.

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Why do we want or need to do this?

- FAA Generic Issue Paper (gen_pld8.doc)
  - •Applied on a project by project basis by the ACO in order to meet FAA FAR 25.1309.
  - •DO-254 or equivalent is required for "complex devices".
- JAA Temporary Guidance Leaflet (TGL)
  - •Applied generically for all projects
  - •requires DO-254 for Levels A, B, C
- Draft AC for DO-254 (generated by GAMA)
  - •Applied generically for all projects
  - • Requires DO-254 for only levels A & B and only if HDL is used?.

The Many Hats We Wear

- Roles in the PLD development process:
  - – Company policy and development process initiator, author and coordinator
  - – "Coach" for the hardware engineers trying to understand the objectives.
  - – FAA DER review and approval of design data for PLDs
- In each of these roles I have lessons learned and success stories to share

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Role 1:Company policy and development process initiator, author and coordinator

- Typical questions asked by hardware engineering:
  - How many documents do we need to make this happen? (i.e. how many trees need to die)
  - Hardware Plans (CM, QA, Verification, Development, etc…) for each new project?
  - What's a PHAC anyway and why do I care?
  - How many more people are they going to hire to do this work?

Role 1:Company policy and development process initiator, author and coordinator

- An approach:
  - Write a company PLD and ASIC development standard which capitalizes on the processes which are already in place but maps into the objectives set forth in DO-254 or DO-178B.
  - This PLD and ASIC development standard is then submitted to the FAA ACO office for approval as an acceptable means for development of ALL (level A-E) devices by the company.

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Role 1:Company policy and development process initiator, author and coordinator

- Pros:
  - Hardware engineers like one document which contains the applicability and implementation specifics for the DO-254 or DO-178B objectives.
  - Approaching the discussion from this perspective: “You are probably already meeting 90% of these objectives, lets figure out together these 90% and write them down, and fill in the holes with what makes sense together.”
  - Hardware engineers can help write and “determine there own destiny”. They are more likely to use the process.
  - The process of writing this helps to gain and understanding of “why” some of these objectives are of value and necessary.
  - FAA has a clear vision of the companies approach and design processes and so does the company!

Role 1:Company policy and development process initiator, author and coordinator

- Cons:
  - Sometimes there are lots of holes to fill (ie. Standard CM, QA and verification activities don’t exist).
  - Hardware engineers may not be familiar with DO-178B or the idea of a “development process”.
  - In several cases, Digital and Analog Hardware engineers are new to PLD and ASIC design and related development tools. They have been pushed into using PLDs and ASICs due to board space, weight, complexity, flexibility, power consumption, speed requirements, etc.
  - Process development can be slow, the education and group consensus process slows down the writing of the PLD and ASIC development Plan.

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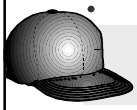
Role 1:Company policy and development process initiator, author and coordinator

- Helpful Hint: Make sure that the PHAC or other planning document includes a table which maps the company standards to the DO-254 or DO-178B objectives (depending on which design assurance guideline the process is based on) See presentation handouts for examples.

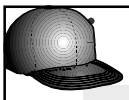


Role 2: "Coach" for the hardware engineers trying to understand the objectives

- If a accepted process exists, not everyone participates in the process development and many times the "why" gets forgotten.
  - Helpful hint: Give real examples of what could go wrong if they don't meet these objectives. This is where having and understanding of the PLD and ASIC development process and tools really helps out.

Role 2: "Coach" for the hardware engineers trying to understand the objectives

- Some typical questions:
  - What do I need to control about the tools I use in the development of a PLD?
  - The tool I use doesn't give me fix checksum for the part, is that important?
  - What testing do I need to do and what documentation is different for a level A PLD vs. a Level C?
  - What is the scope of information in the PHAC and when do you need to submit it to the FAA?
  - Can I use 100% simulation to fully functionally verify my PLD?
  - Do I need to worry about that off-the-shelf Core I put into my FPGA?



Role 2: "Coach" the hardware engineer trying to understand the objectives

- Some typical questions:
  - Can re-use my ARINC 429 receiver FPGA from an already certified product? What do I need for certification?
  - My part has gone obsolete and there is no drop in replacement, I need to re-target my source, what do I need to do to satisfy the FAA? Is this a minor or a major change to the system?
  - I have 4 parts daisy chained together for JTAG programmability, can I just list the daisy chain file in the Configuration Index Document?
  - Can I use my boundary scan feature of JTAG to satisfy the functional testing for the device?
  - We out-sourced the design for this PLD, what documentation do I need?
  - I purchased an Ethernet Custom IC that included in my design, do I need to consider this as a PLD? What about my "Maxim" power monitor chip?

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Role 3:FAA DER review and approval of design data for PLDs

- This job is much easier if there is an existing FAA approved PLD/ASIC development process.
- FAA DER special designation for PLD and ASIC approval.
- Using a review process similar to what is suggested in the Software Job Aid.
- 8110-3 includes PHAC, CID and Accomplishment Summary (or equivalent).

Role 3:FAA DER review and approval of design data for PLDs

- Favorite areas of focus:
  - Configuration Management of the source, design and tools (where most of the scary stuff happens)
    - Always have them rebuild the part and demonstrate the programming process until you have confidence that all areas of this process are documented and accounted for.
    - Look to see if there is evidence of Process Assurance activities associated with changes to the design. Evidence of Process Assurance Engineering having the engineer rebuild and demonstrate programming of the parts for major changes in source and tool version changes.

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Role 3:FAA DER review and approval of design data for PLDs

- Favorite areas of focus: (cont..)
  - Verification coverage and Traceability
    - Many times the hardware designer will take credit for software verification or hardware qual testing activities for the PLD. Verify that the traceability exists and that the software verification or hardware qualification tests have passed and are under CM.
    - Automatic Test Procedures (ATP) for the end item product are sometimes used for verification coverage credit, verify that the ATP tests are run on the same version of the PLD and hardware configuration. (ie. Did they conduct a Test Readiness Review for PLDs?)
    - If verification coverage is been met via software verification test, ATP, or some other source, is there a procedure in place for the maintenance phase of the product to ensure that changes to these tests are assessed for impact to the PLD verification?

Are SW DERs value added in this area?

- DERs with hardware background and/or understanding makes there contribution more valuable.
- The issues which are crucial to PLD/ASIC development relative to determining intended function and conformity are similar to that for embedded software.
- Who else would do it?

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Links to information

- http://av-info.faa.gov/software/complexhdw.htm : FAA info
- http://www.optimajic.com/faq.html :FAQ about PLDs
- http://www.jaa.nl/
- http://www.xilinx.com/ipcenter/index.htm :Xilinx IP Cores
  http://www.altera.com/products/ip/ipm-index.html :Altera IP Cores
  http://www.actel.com/products/ip/index.html :Actel IP cores
  http://www.model.com/ :ModelSim VHDL/Verilog simulation tools
  http://www.synplicity.com/ :Synplicity ASIC/FPGA/CPLD synthesis primarily for FPGA
  http://www.synopsys.com/ :Synopsys ASIC/FPGA/CPLD synthesis primarily for ASIC
  http://www.gnu.org/directory/emacs.html :emacs general editor
  http://opensource.ethz.ch/emacs/vhdl-mode.html#updates :emacs VHDL mode

- DOT/FAA/AR-95/31 - “Design, Test and Certification Issues for Complex Integrated Circuits”.
- The Designer’s Guide to VHDL - by Peter J. Ashenden ISBN 155860-270-4